Amendments to the Claims:

1.   (Currently Amended) A method of performing built-in self repair of memories

comprising:

~~making an on-chip assessment of amount of repair of a memory and flagging any memory~~

~~as a fail when that memory exceeds a pre-determined limit~~

testing the memories a first time;

generating a repair solution;

using the repair solution to repair the memories while flagging those memories whose

repair exceeds a pre-determined limit;

making an on-chip assessment to test the memories a second time; and

using the repair solution to repair the memories which need to be repaired and which

were not previously flagged.

2.   (Original) The method as recited in claim 1, further comprising loading a counter with

one or more values which establish a threshold for pass/fail criteria.

3.   (Original) The method as recited in claim 2, further comprising loading the counter

through a test pattern during production testing.

4.   (Original) The method as recited in claim 1, further comprising loading a pre-determined

repair solution into registers, testing the memories, and thereafter initiating the repair solution to

repair the memories.

5.   (Original) The method as recited in claim 4, further comprising using a reliability controller to test and repair the memories.

6.   (Original) The method as recited in claim 5, said reliability controller comprising logic, at least one counter in communication with said logic, and a register set in communication with said logic.

7.   (Original) The method as recited in claim 6, wherein said at least one counter comprises a first counter which contains the number of memories to be allowed for repair.

8.   (Original) The method as recited in claim 7, further comprising loading a value into the register set which indicates the total number of memories.

9.   (Original) The method as recited in claim 8, further comprising loading another value into the register set which indicates the maximum number of flare register bits among the memories.

10.   (Original) The method as recited in claim 9, further comprising having the logic use the two values to create sections of patterns for each memory.

11.   (Original) The method as recited in claim 10, wherein a start of each section contains redundant usage information.

12.   (Currently Amended) A reliability controller configured for use in connection with built-in self repair of memories, said reliability controller configured to: ~~make an on-chip assessment of amount of repair of a memory and flag any memory as a fail when that memory exceeds a pre-determined limit~~

test the memories a first time;

generate a repair solution;

use the repair solution to repair the memories while flagging those memories whose repair exceeds a pre-determined limit;

make an on-chip assessment to test the memories a second time; and

use the repair solution to repair the memories which need to be repaired and which were not previously flagged.

13.   (Original) The reliability controller as recited in claim 12, said reliability controller comprising logic, at least one counter in communication with said logic, and a register set in communication with said logic.

14.   (Original) The reliability controller as recited in claim 13, wherein said at least one counter comprises a first counter which contains the number of memories to be allowed for repair.

15. (Original) The reliability controller as recited in claim 14, wherein the register set is configured to receive a value which indicates the total number of memories.

16. (Original) The reliability controller as recited in claim 15, wherein the register set is configured to receive a value which indicates the maximum number of flare register bits among the memories.

17. (Original) The reliability controller as recited in claim 16, wherein the logic is configured to use the two values to create sections of patterns for each memory.

18. (Original) The reliability controller as recited in claim 17, wherein a start of each section contains redundant usage information.